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The Fairchild F8 Kit will permit you to build with a minimum number of parts a complete F8 Microprocessor system.

1) Kit Description:

The following parts are included:

1 - 3850 F8 CPU
1 - 3851A F8 PSU Preprogrammed FAIR-BUG ROM
1 - 3853 F8 MI
8 - 21022 1K MOS RAM
2 - 340097 CMOS Buffer
1 - 34001 CMOS Quad NOR
1 - 34023 CMOS Triple NAND
1 - 9N06 TTL HEX Invert.

2) Kit Features:

The F8 Kit assembled as indicated by the schematic drawing will provide the following features:

- 1024 bytes of program or data storage at address H'0000' to H'03FF'
- 4 I/O Ports having the following addresses:

  3850 CPU I/O: H'00'
  H'01'

  3851 PSU I/O: H'04'
  H'05'

  All I/O Ports are the standard configuration suitable for TTL interface.

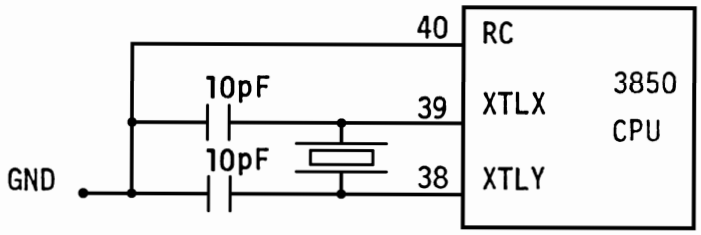
- 2 levels of interrupt:

  The first level is provided by the 3851 PSU. It has the highest priority being the first in the priority chain. Its vector address is fixed at H'0010' for timer interrupt and H'0090' for external interrupt. The port address, for local interrupt control is H'06'. The port address for the timer is H'07'.

The second level is provided by the 3853 MI. It has the lowest priority being last in the priority chain. Its vector address is programmable. The following Port and functions are as follows:

Port Address	Function
H 'OC'	Interrupt vector upper byte
H 'OD'	Interrupt vector lower byte
H 'OE'	Local Interrupt Control
H 'OF'	Timer

- The clock reference frequency circuit shown on the schematic drawing is of the R.C. type. Using the values indicated C = 10 pF and R = 25 KΩ adjustable, a clock frequency in the range of 1.0 to 2 MHZ can be selected. If a more accurate operating frequency is required, an external crystal may be used to select a frequency. Crystal connections are shown below:



An external clock can also be used as reference frequency by connecting clock signal to PIN 38 and GND to PIN 40.

- External Reset: Using a momentary switch connected as indicated, external reset or program restart at zero can be initiated manually.

  In the DEBUG Mode as explained further under FAIR-BUG, the "RESET" function causes an entry in the Debug program instead of a program restart at zero.

- Teletype Interface: A teletype convertor circuit is shown as part of the F8 Kit schematic. This circuit permits to easily interface with a Teletype Model 33 teleprinter, it provides signals for 4 wire full duplex, 20 MA current loop. The recommended teletype is a Teletype Model 33 ASR with

automatic reader on/off control. See Appendix F for Strapping options and other TTY interfaces. Output data to the TTY is taken from bit Ø of I/O port 4. Input data from the keyboard is input to bit 7 of I/O port 4. A teletype MARK is a logic 1 (A Ø volt level at the I/O port). Baud rate is a function of the software program and can be selected by stapping bit 1 and 2 of I/O port 4 (See Input/ Output section of FAIR-BUG). The connection shown on the Kit schematic diagram (I/O port 4, bit 1 & 2 = Open) correspond to a 110 baud rate or 10 CPS.

- Debug Program (FAIR-BUG):

INTRODUCTION

A special Debug ROM 3851A PSU has been developed by Fairchild to provide the F8 Kit user with a convenient and powerful programming debut facility which is used to aid in the development of software on the F8 Kit. This debugging program (FAIR-BUG) provides the user with an interactive system via a teletype terminal. The following capabilities are provided:

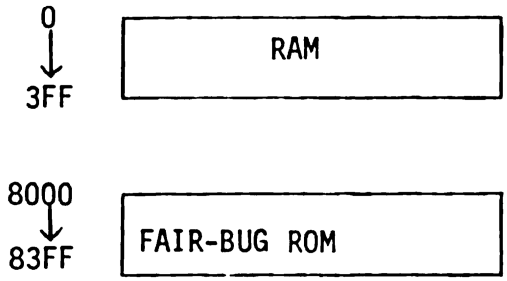
Display or Alter Memory Locations
Display or Alter Scratchpad Registers
Display or Alter Accumulator, ISAR, Status (W Register)
Display or Alter PC0, DC0, DC1
Load Formatted Paper Tape
Punch Formatted Paper Tape
Punch Paper Tape in PROM format
Entry from Keyboard or by Program Instruction
I/O Subroutines available to user

The FAIR-BUG ROM has the memory addresses 8000 - 83FF with the entry point being H'8080'. Input/Output Ports 4 and 5 are also assigned to this ROM. Entry to the debug program is achieved either by depressing the "RESET" switch with the Mode Switch "DEBUG" in the "ON" position or by program instruction PI H'8080'.

FAIR-BUG will save the state of the machine upon entry and will restore it upon return to the users program. Register 8 and PC1 are lost by the system; however, under program control the user can save and restore these if necessary. The save area utilized by FAIR-BUG is scratchpad registers 3C to 3F and also the last 26 bytes of RAM whose address will either be 3E6 to 3FF or BE6 to BFF. The interrupt is disabled by FAIR-BUG which the user may re-enable if desired.

MEMORY ALLOCATION

The basic F8 Kit system contains 1024 bytes of memory which may be expanded by the user. This memory is organized as shown below:



The FAIR-BUG uses the last 26 bytes of RAM to save the users CPU status. This is address: 3E6 to 3FF

INPUT/OUTPUT

The FAIR-BUG ROM has 2 ports (4 & 5) which are also available to the user when FAIR-BUG is not executing.

Port 4 is used for serial input/output and control functions while Port 5 is used for parallel input data transfer from a high speed paper tape reader. Assignments for Port 4 are:

Bit	Function
7	Serial input
6	Character Ready (Parallel Device)
5	---
4	Device Ready (Parallel Device)
3	Step Reader (Parallel Device)
2 - 1	See table below

bit 2	bit 1	Teletype Baud Rate	Input source during tape load
0	0	110 baud	teletype
0	1	300 baud	teletype
1	0	Baud delay in memory (location 3FF or BFF)	parallel source (port 5)
1	1	Baud delay in memory	teletype

0 = Open
1 = GND

Serial Output

If Port 5 is not utilized by FAIR-BUG, then bits 3, 4, and 6 of Port 4 are also available to the user.

FAIR-BUG parallel read routine examines DEVICE READY and waits for the ready signal, it then looks for Character Ready and delays 100μsec after detecting the ready, then it reads a character before the output of Step Reader. This sequence is repeated for each character. Only the format shown in Appendix B can be read by FAIR-BUG with the Load command. However, the user may use the subroutine PINP to read other formats.

Bits 1-2 are examined when FAIR-BUG is entered to initialize the baud delay counter and also whenever a Load command is given to determine whether the input is bit serial or parallel on Port 5.

FAIR-BUG COMMANDS

When FAIR-BUG is entered a prompt character (?) is sent to the output device. The user then has the option of using any of the debug commands. After each debug execution the user is again prompted with (?). All data and input parameters are in hexidecimal notation. (C/R) following a command indicates a carriage return.

COMMAND TYPE	COMMAND	FUNCTION
Display	A (C/R)	Display the contents of the Accumulator
	DO (C/R)	Display the contents of DCO
	D1 (C/R)	Display the contents of DC1
	I (C/R)	Display the contents of ISAR
	M XXXX (C/R)	Display Memory Location XXXX
	M XXXX-YYYY (C/R)	Display Memory Location XXXX to YYYY
	PO (C/R)	Display the contents of PCO
	P1 (C/R)	Display the contents of PC1
	R XX (C/R)	Display the contents of Register XX
	R XX-YY (C/R)	Display the contents of Registers XX to YY
	S (C/R)	Display the contents of W Register, status
	W (C/R)	Display the contents of W Register, status
Change	C XX (C/R)	Change the previously displayed memory location or register to XX
	C XXXX (C/R)	Change the previously displayed PC or DC to XXXX
Examine	E (C/R)	Display the last addressed register or memory location
Next	N (C/R)	Display the next register or memory location
Load	L (C/R)	Load formatted object paper tape. If (CK) prints then checksum error has occurred on block last read
Punch	B XXXX-YYYY-Z	Binary Punch PROM format XXXX is starting page address and YYYY is ending page address. Z is number of bytes per block 0 = 256, 1 = 512. To punch 0 to BFF then enter B0-C00-0.

COMMAND TYPE	COMMAND	TYPE
	F XXXX-YYYY (C/R)	Formatted punch for future load Manually turn punch to "ON" before issuing the CR .
Go To	G (C/R)	Go to address of PCO
	G AAAA (C/R)	Change PCO to address AAAA, then go to AAAA to execute next instruction
Delete Command	[	Delete command and start a new command input string

I/O Subroutines on the FAIR-BUG ROM are available to the user. These are listed below and documented in Appendix C.

NAME	ENTRY ADDRESS	FUNCTION
TTYI	83AD	Input 1 byte from TTY type device (11 bits serial/character)
TTYO	83E5	Output 1 byte to TTY type device (11 bits serial/character)
TTCR	83E4	Output CR, LF & Null characters using TTYI subroutine
PINP	8397	Input 1 byte from the parallel IP device (150μsec minimum delay between characters)
FOP1	80EC	Output 1 or 2 hexidecimal digits in ASCII format from register QL
FOP2	80EE	Output 1 or 2 hexidecimal digits in ASCII format from a memory location
BYTE	837B	Input 2 ASCII characters from a parallel or serial IP device; then convert them to one hexidecimal byte

APPENDIX A

FAIR-BUG EXAMPLE 1

```
?M0
 M0000=00
?C 70
?N M0001=91
?C 0B
?N M0002=00
?C 5C
?N  M0003=DD
?C 1F                    STORE A PROGRAM TO SET
?N M0004=04              SCRATCHPAD TO 0-3F.
?C 25
?N M0005=10                     LIS 0
?C 3F                    LOOP   LR  IS,A
?N M0006=00                     LR  S,A
?C 94                           INC
?N CF9 M0007=D1                 CI  H'3F'
?C F9                           BNZ LOOP
?N M0008=00                     JMP H'8080'
?C 29
?N M0009=10
?C 80
?N M000A=00
?C 80
?M0-A
 M0000=70 0B 5C 1F 25 3F 94 F9   DISPLAY PROGRAM
 M0008=29 80 80 D0 00 10 00 91
?R0-3F
 R0000=A4 FF 09 FF 00 00 FF 00
 R0008=83 0A 00 FF 81 97 03 FF
 R0010=0C 20 13 00 1E 00 BF 00   DISPLAY SCRATCHPAD
 R0018=9D 40 7D 01 DD 17 55 00   BEFORE EXECUTION
 R0020=B7 F7 7F A2 FF 0E FF 22
 R0028-FF 76 FF 3C FF CE 5F 20
 R0030=18 04 02 00 D9 04 7F 00
 R0038=75 01 57 4A  F 0A 0A FF
?G0                              GO TO LOC 0 TO EXECUTE
?M7                              (PROGRAM LOOP ERR.) MANUAL RESET TO FAIRBUG
 M0007=F9
?C FA                            CORRECT BNZ INSTRUCTION
?G0                              GO TO 0
?R0-3F
 R0000=00 01 02 03 04 05 06 07
 R0008=80 09 0A 0B 0C 0D 0E 0F   DISPLAY REGISTERS AFTER
 R0010=10 11 12 13 14 15 16 17   EXECUTION.
 R0018=18 19 1A 1B 1C 1D 1E 1F   NOTE: R8, R3C-3F ARE USED
 R0020=30 21 22 23 24 25 26 27   BY FAIRBUG.
 R0028=28 29 2A 2B 2C 2D 2E 2F
 R0030=30 31 32 33 34 35 36 37
 R0038=38 39 3A 3B 3E 09 09 0B
?P0 0000                         PC NOT SAVED BY JMP.
?P1 EEEE
?M8
 M0008=29                        CHANGE JMP TO P1
?C28
?G0                              EXECUTE AGAIN
?P0 000B                         PC NOW SAVED!
?
```

APPENDIX A

FAIR-BUG EXAMPLE 2

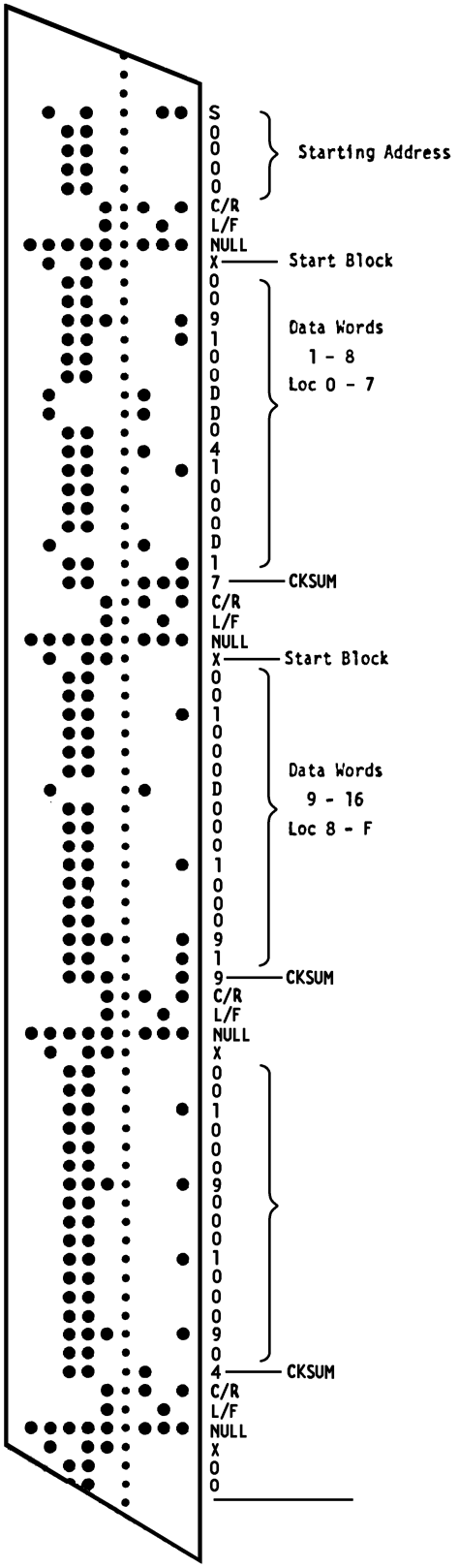
```
 R5
 R0005=00
?R1-2
 R0000=A4 FF 09 00 00 00 FF 00      R1-2 TYPES R0-R7
?N R0008=83                         NEXT=R8
?C55                                CHANGE R8 TO 55
?E R0008=55                         EXAMINE R8
?R8
 R0008=55
?P0 83B0
?D0 807B
?D1 0000
?CFFFF                              DISPLAY DC1, CHANGE, EXAMINE,
?E FFFF                             THEN DISPLAY AGAIN
?D1 FFFF
?I=0F                               ISAR
?S=0A                               STATUS
?W=0A
?M3E0-3FF
 M03E0=04 00 00 10 00 00 00 83
 M03E8=B0 EE EE 80 7B FF FF A4      MEMORY DUMP
 M03F0=FF 09 00 00 00 FF 00 55
 M03F8=0A 00 FF 81 97 03 FF 00
?R0-F
 R0000=A4 FF 09 00 00 00 FF 00      REGISTER DUMP
 R0008=55 )A 00 FF 81 97 03 FF
?R10-40
 R0010=00 20 13 00 1E 00 BF 00
 R0018=9D 40 7D 01 DD 17 55 00
 R0020=B7 F7 7F A2 FF 03 FF 22      REGISTER DUMP
 R0028=FF 76 FF 3C FF CE 5F 20
 R0030=18 04 02 00 D9 04 7F 00      NOTE: R40-R47 IS FAIRBUG USE
 R0038=75 01 57 4A 0F 0A 0A FF
 R0040=A4 FF 00 00 44 00 47 EF
?B0-100-00F0B0N0B0N0B0N0F0M0F0N0F000BNN0BMBM@0@0@M@0CM@M@M@0@MA0@MB0@0FM@NN0BL
                                    PUNCH FORMAT (PROM TAPE)
                                    SEE APPENDIX C FOR FORMAT
?F0-FFS0000                         PUNCH FORMAT (LOAD TAPE)
X009100DD041000D17
X001000D0001000919
X0010009000100090 4
X000000D1141002D47

                                    SEE APPENDIX B FOR FORMAT
X24DA20C1AFFB20FFF
X26C802F3268164FBD
X20D900FF24F900F9C
X26F900FF2ED92EF58
*                                   * (END OF TAPE)
?F0-FF
?A=83                               DISPLAY, CHANGE, EXAMINE ACCUMULATOR
?C00
?E R0008=00
?N R0009=0F                         NOTE:  ACCUMULATOR IS IN R8  THEREFORE NEXT IS R9
?G8080                              GO TO 8080
?PC 00FF
?P0 8080                            PC0 CHANGED TO 8080
?G                                  GO TO PC0 (8080)
?
```

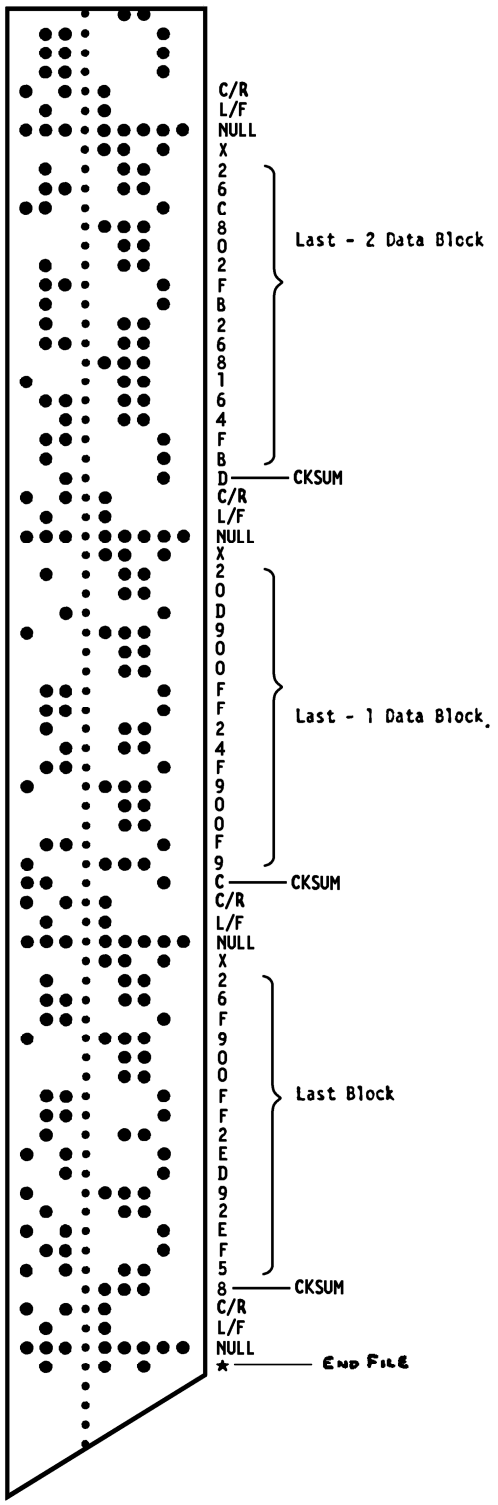
APPENDIX B

FORMATTED TAPE

(LOADER FORMAT)



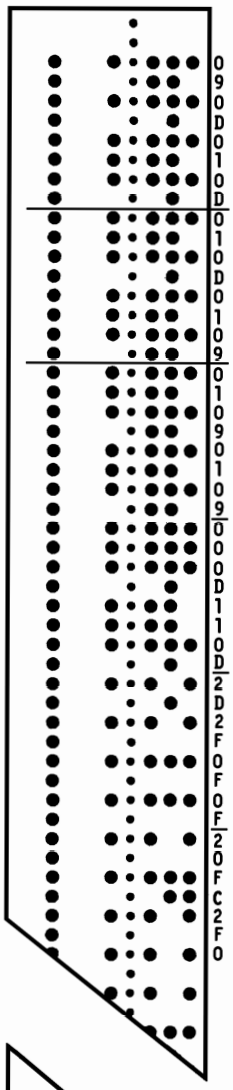
Note: This example was punched by the instruction shown in Appendix B (F0-FF). This is ASCII 7 bit format.

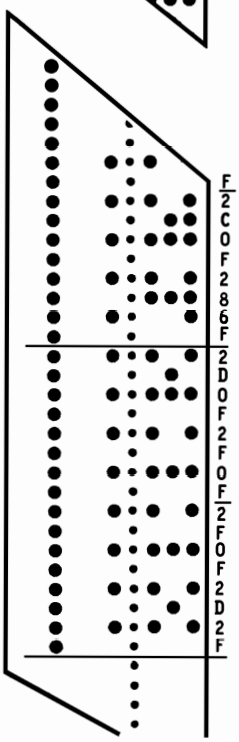


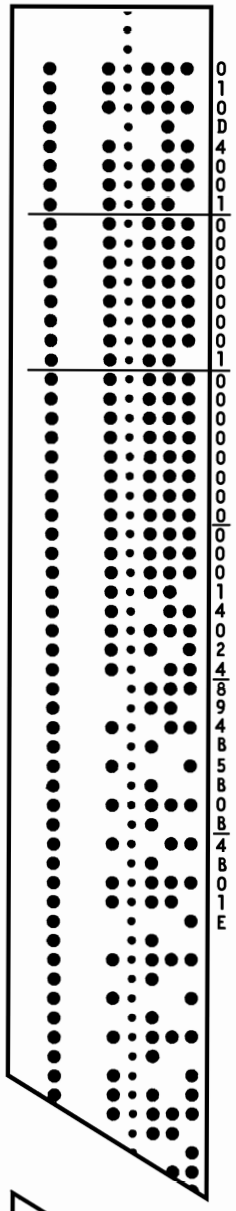
APPENDIX C

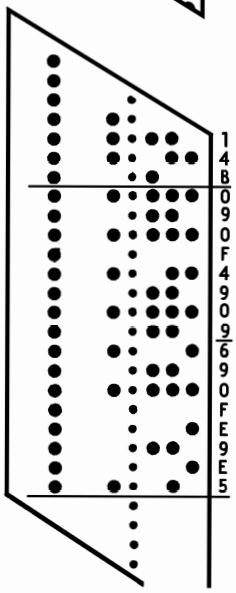
BINARY FORMAT

(PROM GENERATION FORMAT)









Note: This example was punched by the instruction shown in Appendix B (B-100-0).

Only the low order 4 bits are significant and are punched in compliment form.

The first block is punched with 256 memory locations hi order bits. The next block has 256 memory locations low order bits.

Subsequent blocks then alternate hi, low, hi, low, etc. with a blank gap between.

The table below shows examples of commands and the results produced.

Input Command B-XX00-YY00-L	Decimal Memory Addresses Punched	# Blocks	Block Length
B 0-100-0	0-255	2	256
B 0-400-0	0-1023	8	256
B 100-200-0	256-511	2	256
B 0-400-1	0-1023	4	512
B 0-1000-1	0-4095	16	512
B 200-400-1	512-1023	2	512

APPENDIX D
FAIR-BUG SUBROUTINES

The following INPUT and OUTPUT subroutines exist in FAIR-BUG and may be called by the users program. All subroutines may be entered by: (PI Address).

TTYI - Input 1 byte from TTY type device, without echo. Data is 11 bits/character being received on Port 4 Pin 7.

```
Address:  H'83AD'
Enter:    R0 - Delay Counter
Exit:     W Reg - Destroyed
          PC1 - User return address
          Accum - Input byte
          R0 - Unchanged
          R1 - Input byte
          R2 - -1
```

TTYO - Output 1 byte to TTY type device. Data transmitted is 11 bits/character being output on Port 4 Pin 0.

```
Address:  H'83E5'
Enter:    R0 - Delay Counter
          R1 - Byte to output
Exit:     W Reg - Destroyed
          PC1 - User return address
          Accum - 0
          R0 - Unchanged
          R1 - -1
          R2 - 0
```

TTCR - Output CR/LF/NULL to TTY type device; subroutine TTYO is called.

```
Address:  H'83D6'
Enter:    R0 - Delay Counter
Exit:     W Reg - Destroyed
          PC1 - H'83E4'
          Accum - 0
          K Reg - User return address
          R0 - Unchanged
          R1 - -1
          R2 - 0
```

PINP - Input 1 byte from parallel input device; minimum delay between characters is 150μsec. Byte is received on Port 5 with control bits on Port 4, pins 3, 4, and 6.

```
Address:  H'8397'
Enter:    No setup
Exit:     W Reg - Destroyed
          PC1 - User return address
          Accum - Input byte
          R1 - Input byte
```

BYTE - Input 2 ASCII hexidecimal characters and convert to 1 byte; also accumulate the checksum. If input is not ASCII characters 0-9 or A-F meaningless results will be returned. Either TTYI or PINP is called as input routine.

```
Address:  H'837B'
Enter:    Q - H'8397' (for parallel input)
          Q - H'83AD' (serial input) R0 = Delay Counter
          R7 - Previously accumulated checksum
Exit:     W Reg - Destroyed
          PC1 - Destroyed
          Accum - Input byte
          K - User return address
          Q - Unchanged
          R0 - Unchanged
          R1 - Destroyed
          R2 - -1 (if serial IP), unchanged for parallel IP
          R7 - Checksum
          R8 - 0
          R11 - Input byte
```

FOP1 - Output byte of data from memory to TTY type device using TTY0 subroutine. Byte is converted to 1 or 2 ASCII hexidecimal characters.

```
Address:  H'80EC'
Enter:    R0 - Delay Counter
          R8 - Flag Pos# = OP Hi 4 bits, then Lo 4 as ASCII
                    Neg# = OP Lo 4 bits as ASCII
          DC0 - Memory address of data
Exit:     W Reg - Destroyed
          PC1 - Destroyed
          Accum - Destroyed
          DC0 - DC0 + 1
          K Reg - User return address
          QL - Data byte
          R0 - Unchanged
          R1 - -1
          R2 - 0
          R7 - Checksum (low 4 bits significant)
```

FOP2 - Output byte of data from QL. Same routine as FOP1 except DC0 is not used.

```
Address:  H'80EE'
Enter:    R0 - Delay Counter
          R8 - Same as FOP1
          QL - Data byte to output
Exit:     Same as FOP1
```

APPENDIX E

ASCII CHARACTER CODES

Character	7 Bit Hex Code	Character	7 Bit Hex Code	Character	7 Bit Hex Code
(Space)	20	0	30	H	48
!	21	1	31	I	49
"	22	2	32	J	4A
#	23	3	33	K	4B
$	24	4	34	L	4C
%	25	5	35	M	4D
&	26	6	36	N	4E
' (Quote)	27	7	37	O	4F
(	28	8	38	P	50
)	29	9	39	Q	51
*	2A	:	3A	R	52
+	2B	;	3B	S	53
, (Comma)	2C	>	3C	T	54
-	2D	=	3D	U	55
.	2E	<	3E	V	56
/	2F	?	3F	W	57
		@	40	X	58
		A	41	Y	59
Line Feed	0A	B	42	Z	5A
Carriage RTN	0D	C	43	[	5B
Bell	87	D	44	\	5C
Punch ON	92	E	45	]	5D
Punch OFF	94	F	46	↑	5E
Reader ON	91	G	47	←	5F
Reader OFF	93				
Null	7F				
Null	FF				

APPENDIX F: Connecting a Teletype Model 33

The F8 Kit system can easily interface with a Teletype Model 33 teleprinter. The teletype convertor of the micromodule provides signals for a 20 mA full duplex loop.

The recommended teletype is a Teletype Model 33 ASR with automatic reader on/off control. Other Model 33 Teleprinters can also be used.

Teletype Strapping Options

No modifications of the teletype are necessary. Strapping options should be selected to provide 20 mA loop currents in place of 60 mA loops, and to provide full duplex operation in place of half duplex operation. The options are described in the following paragraphs:

1. Parts location: All option points are on the teletype power supply assembly. The power supply assembly is rightmost in the teletype; prominent are the LINE/OFF/LOCAL switch in the front of it, and a row of three fuse holders in the rear. Changes are made on a ten terminal strip (part #151411) that is at the lower rear of the power supply assembly. The other change is made on a large flat multi-tap power resistor (part #181816) that is about three inches behind the LINE/OFF/LOCAL switch.

2. Select 20 mA loop currents by performing Note 2 of the TTY Drawing Number 6353WD which states: "For the .020 amp neutral signal line move the purple wire from Terminal 8 to Terminal 9 of the 151411 terminal strip. Also move the blue wire from Terminal 3 of the power resistor 181816 to Terminal 4."

3. Select full duplex operation by performing Note 3 of TTY Drawing Number 6353WD which states: "Move the white-blue wire from Terminal 4 to 5 and the brown-yellow wire from Terminal 3 to 5 on the 151411 terminal strip."

   Caution: The 110V line cord terminates on the terminal strip. Unplug power cord from the AC source before working on the teletype.

Teletype Model 33 machines provide two alternative places for attaching an interface cable. One location is the 10 terminal strip that is at the rear of the power supply assembly (the same place as where the option changes were made). The optional location is at the 15 pin connector #2 which is just above the terminal strip. One mating plug for connector is:

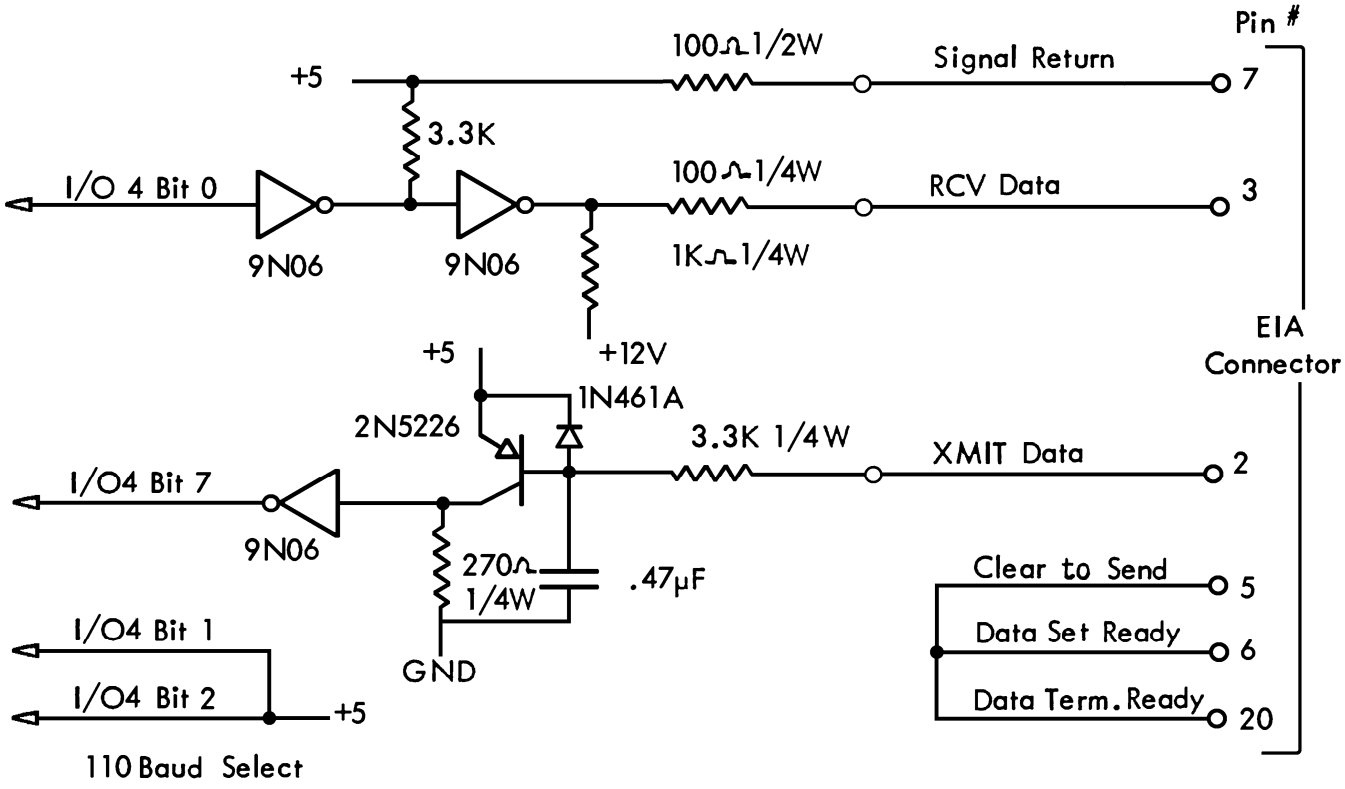
MOLEX part # P(03-09-2151) housing
with MOLEX part # (02-09-2118) terminals

The connections between Teletype and micromodule are:

Teletype	F8 Kit
TS-4 or J2-6	Keyboard
TS-3 or J2-5	Keyboard Return
TS-7 or J2-8	Printer
TS-6 or J2-7	Printer Return

EIA INTERFACE

The following schematic shows alternate TTY convertor circuit for interface with an EIA connector.



APPENDIX H - F8 DESIGN EVALUATION KIT
ASSEMBLY & INSTALLATION OF PC BOARD

The PC board supplied with the kit will make it quick & convenient to get your evaluation kit on the air.

1.0 Documents Supplied

- Fairchild F8 Kit 1 schematic - Rev. C: same as Rev. B except the pin numbers of the PC layout have been added.
- Fairchild F8 Kit 1 assembly drawing.
- Fairchild F8 Kit 1 parts list.

2.0 Assembly

- The PC board is ready for soldering. All IC's are supplied with the kit except for the optional Q6. The discrete parts that you will need to supply are noted on the parts list.

3.0 Options

- There are two areas of option: memory select & TTY circuit select.

3.1 The memory select option choices are:

1) If only the 1K RAM of the kit will be used:
   a) connect strap J1 to ground CE.
   b) Do not install Q6.

or 2) If additional memory will be cabled into the kit board:
   a) Do not strap J1.
   b) Install chip Q6 so that the RAM only responds to addresses H'0000 - H'03FF (strap J1 is located near Q4).

3.2 The TTY circuit option involves straps J2, J3 & J4 & resistors R19 & R20. The option choices are an interface to 20 mA current loop or an interface to RS-232 devices. Figure 1 shows the circuit connected for each of the options. Note that the RS-232 option has the RS-232 signal return at 5 volts above kit ground - in some cases it will be necessary to "float" the kit power supplies when using the RS-232 option.

ERRATA APPLIED

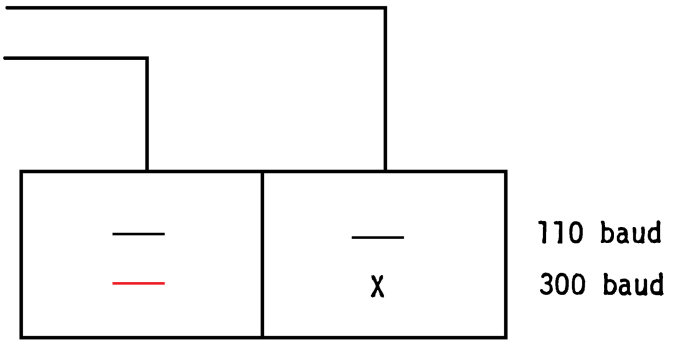
4.0 Installation

The F8 Kit has 4 sets of 8 bit I/O ports. These 32 pins plus two interrupt inputs are brought out to a standard double sided 22 pin PC edge connector (44 connections total). Also on the connector are the power supply voltages & the teletype adaptor connections. Table 1 gives the pin assignments for the connector. The connector is: Amphenol 225-2221-401 or equivalent.

4.1 Power Requirements: +12v ± 5% @ 50mA max - pin N
+5v ± 5% @ 1 Amp max - pin A
GND —— - pin Z

4.2 Teletype Connections: The ttl level signals must be tied to I/O port 4 of the 3851A PSU the 44 pin connector:

connector pin 10 to pin 14
pin 12 to pin 15
pin 16
pin 17



(— = open; x = tie to gnd; see page 5 for other options)

Connections to the teletype are:

Teletype	Name	Kit Connection
TS-4 or J2-6	Keyboard	pin 13
TS-3 or J2-5	Keyboard Return	pin 1
TS-7 or J2-8	Printer	pin M
TS-6 or J2-7	Printer Return	pin 2

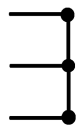
Teletype should be strapped for 20 mA full duplex operation -- this is the strapping most commonly encountered. See Appendix F for teletype strapping instructions & teletype connector locations.

System operating speed should be set to 2.0 MHz ± 5% (500 ns period) for correct teletype operation; monitor the 3850 pin 1 while adjusting pot R4.

ERRATA APPLIED

4.3 RS-232 Connections

RS-232 connection	Name	Kit Connection
7	Signal Return	M (PNTR)
3	Received data	2 (PNTR RTRN)
2	Xmit data	13 (KYBRD)
pin 5	Clear to send	———
6	Data set ready	———
20	Data terminal ready	———



4.4 Memory Expansion Connection

Large pads are provided on one end of the PC board that give access to signals needed to expand the RAM by adding additional 2102 memory banks. The signals available are:

16 bits of ADDRESS:	AD0 - AD15
8 bits of WRITE data:	P1 - P8
8 bits of READ data:	DB0 - DB7
CHIP ENABLE not:	P9
READ/WRITE:	P10

5.0 Operation

The operating controls are the pushbutton RESET switch (S1) and the toggle DEBUG switch (S2).

To enter FAIR-BUG operating system, put toggle switch towards the RESET switch, then push & release RESET (toggle switch closed).

To start a program from RAM location 0000: put toggle switch away from RESET switch, then push & release RESET (toggle switch open).

TABLE 1

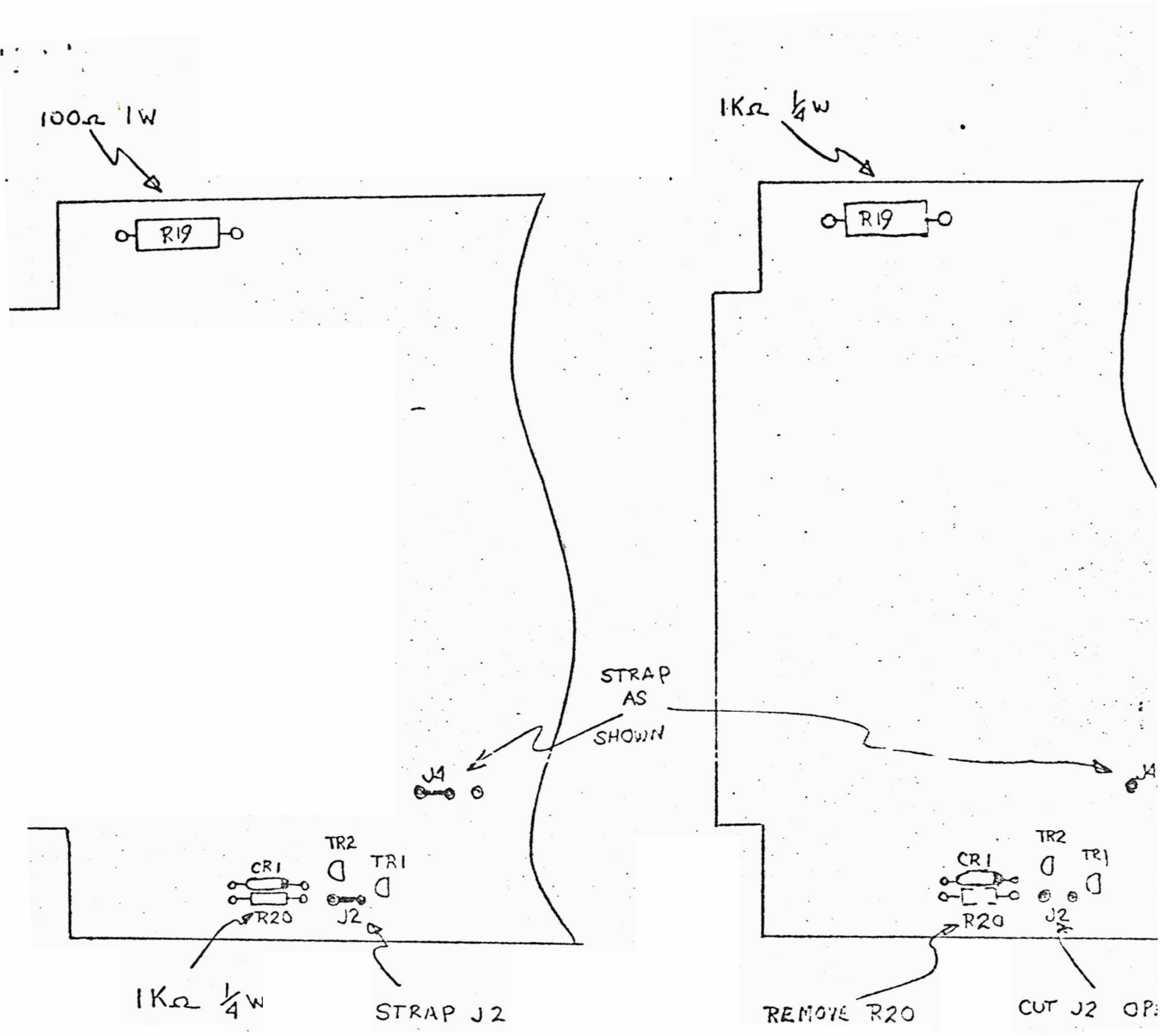
Pin Assignments - Kit Edge Connector

1.	TTY KYBD RTRN	A	+5 volts
2.	TTY PNTR RTRN	B	
3.	I/O 13N	C	I/O 03N
4.	I/O 12N	D	I/O 02N
5.	I/O 11N	E	I/O 01N
6.	I/O 10N	F	I/O 00N
7.	I/O 17N	H	I/O 07N
8.	I/O 16N	J	I/O 06N
9.	I/O 15N	K	I/O 05N
10.	TTY serial input	L	I/O 14N
11.	I/O 04N	M	TTY PNTR
12.	TTY serial output	N	+12 volts
13.	TTY KYBD	P	I/O 57N
14.	I/O 47N	R	
15.	I/O 40N	S	I/O 50N
16.	I/O 41N	T	I/O 51N
17.	I/O 42N	U	I/O 52N
18.	I/O 43N	V	I/O 53N
19.	I/O 44N	W	I/O 54N
20.	I/O 45N	X	I/O 55N
21.	I/O 46N	Y	I/O 56N
22.		Z	Ground

TABLE 2 (J2)

PIN ASSIGNMENTS- 44 PIN CONNECTOR

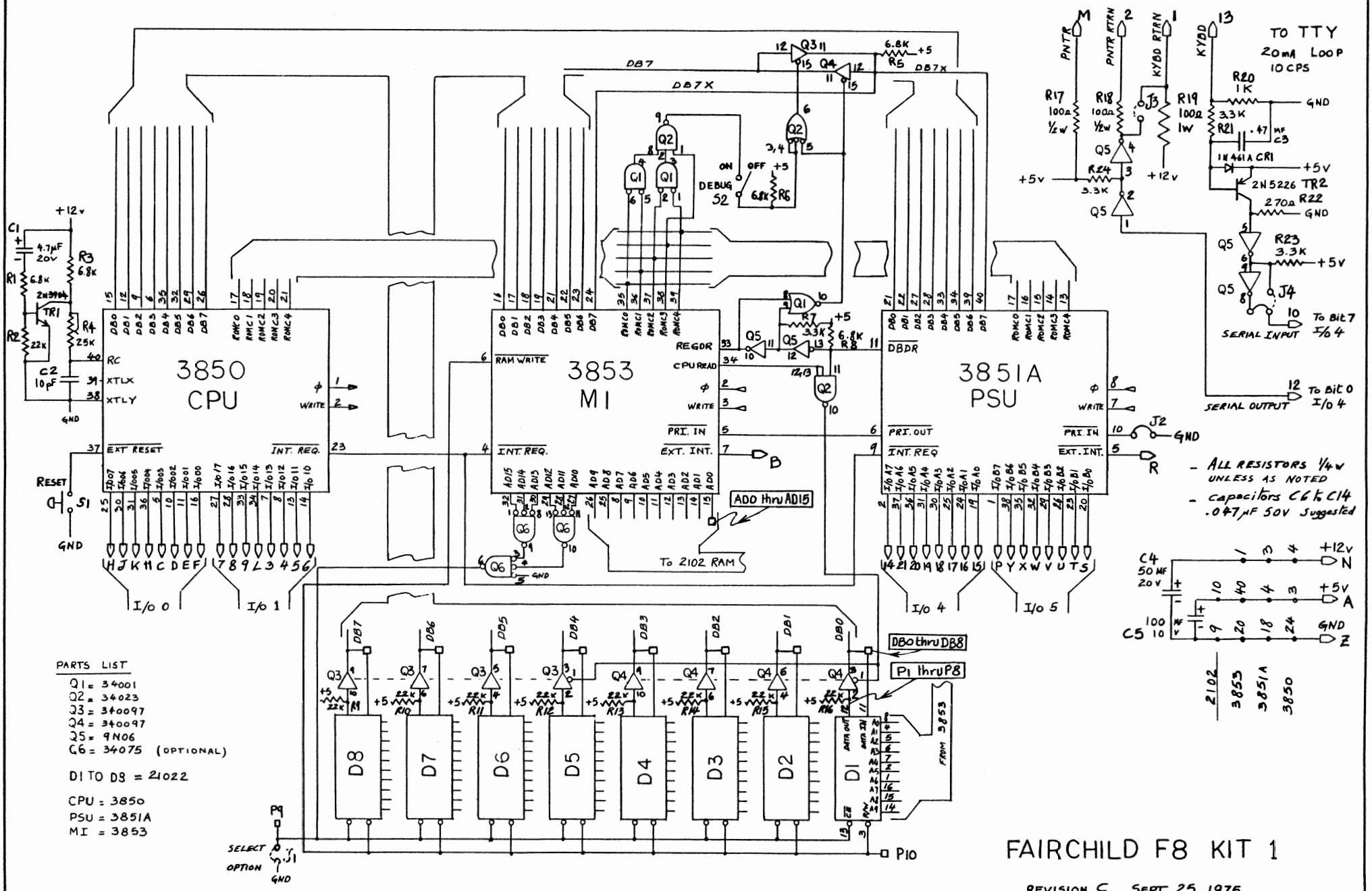
1.		A	
2.	D.B.-7	B	D.B.-6
3.	ADD-14	C	ADD -0
4.	P-8	D	ADD-12
5.	P-6	E	D.B.-5
6.	P-7	F	ADD-15
7.	ADD-11	H	DB-7
8.	ADD-5	J	P-5
9.	P-10(READ/WRITE)	K	D.B.-4
10.	ADD-3	L	ADD-2
11.	ADD 10	M	D.B.-3
12.		N	P-4
13.		P	ADD-7
14.		R	ADD-6
15.		S	ADD-8
16.		T	ADD-9
17.		U	P-3
18.		V	D.B.-2
19.		W	
20.	ADD-1	X	P-2
21.	P-1	Y	D.B.-1
22.	D.B.-0	Z	ADD-3



FOR 20 mA

FOR RS-232

Figure 1 - TTY options



PARTS LIST

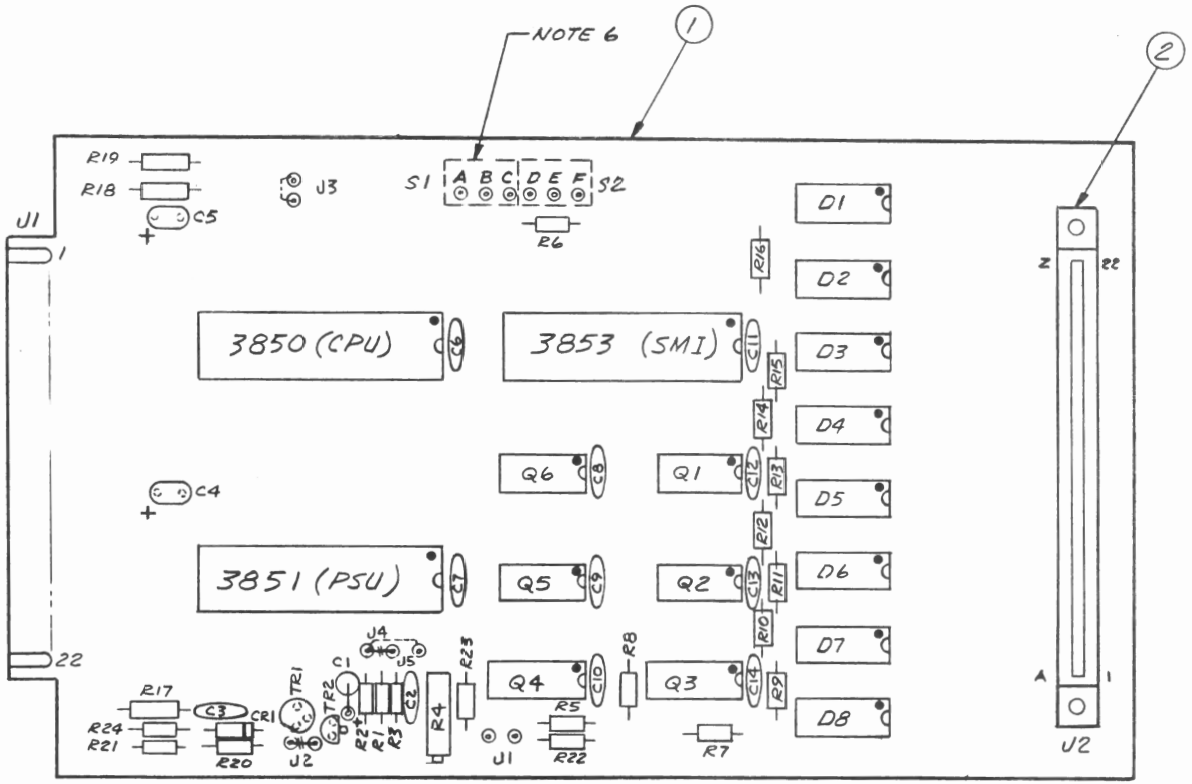
Q1 = 34001
Q2 = 34023
Q3 = 340097
Q4 = 340097
Q5 = 9N06
Q6 = 34075 (OPTIONAL)

D1 TO D8 = 21022

CPU = 3850
PSU = 3851A
MI = 3853

FAIRCHILD F8 KIT 1

REVISION C, SEPT 25, 1975



Fairchild / Mostek F8 Evaluation Kit ('F8 KIT 1' Revision C, Sept 25, 1975)

VERAS SYSTEMS CPU BOARD ASSY

PARTS LIST

ITEM NO.	PART IDENT	QTY	ITEM NO.	PART IDENT	QTY	ITEM NO.	PART IDENT	QTY
Q6	4075	1	1	VERAS CPU BD.	1	D1-D8	2102-1<500NS	8
Q5	7406	1	2	CONNECTOR, 22 PIN DUAL	1			
Q3&6	40097	2	C4	47μf/35V TANT	1			
Q1	4001	1	C5	150μf/15V TANT	1			
Q2	4023	1	C6-C14	.05μf/50V DISC	9			
TR1	2N3638	1	R1,3,5,6&8	6.8K, ¼W RES	5			
TR2	2N3904	1	R2,R9-16	22K, ¼W RES	9			
CR1	1N4148	1	R4	35K HELIPOT	1			
C1	4.7μf/35V TANT.	1	R7,21,23&24	3.3K, ¼W RES	4			
C2	10Pf/25V DISC	1	R17-R19	100Ω, ½W RES	3			
C3	.47μf/35V TANT	1	R22	270Ω, ¼W RES	1			

NOTES:

1.) THE CPU BOARD IS SHOWN ASSEMBLED FOR INTERFACING WITH A 20 MA LOOP. IF AN RS-232 INTERFACE IS REQUIRED THEN THE FOLLOWING MODIFICATIONS MUST BE MADE:
(A) CUT JUMPERS J2 & J4 OPEN (B) ADD JUMPER J3 & J5 SHOWN WITH DOTTED LINES ON DWG.
(C) REMOVE R19(100Ω 1/2W) & REMOVE R20 (1KΩ 1/4W) SUBSTITUTE R20 IN PLACE OF R19.
THE RS-232 SIG RTN IS AT 5 V ABOVE KIT GND, IN SOME CASES IT WILL BE NECESSARY TO "FLOAT" THE KIT PWR SUPPLIES WHEN USING THE RS-232 INTERFACE.

2.) SYSTEM OPERATING SPEED SHOULD BE SET TO 2.0 MHz ±5% (500NS PERIOD) FOR CORRECT TELETYPE OPERATION; ADJUST POT R4 WHILE MONITORING PIN 1 ON THE 3850 CPU.

3.) SOME COMPONENTS HAVE BEEN SUBSTITUTED AT VERAS SYSTEMS DISCRETION BUT THIS WILL NOT EFFECT THE PROPER OPERATION OF THE CPU BOARD.

4.) USE OF A LOW POWER SOLDERING IRON & A GOOD GRADE OF 60/40 ELECTRONIC SOLDER IS A MUST.

5.) AFTER ALL COMPONENTS ARE SOLDERED, CHECK FOR SOLDER BRIDGES & COLD SOLDER JOINTS.

6.) IF THE CPU BOARD IS CARD RACK MOUNTED, DO NOT INSTALL S1&S2 (SEE SYSTEMS WIRING DIAG.)

7.) ● DENOTES PIN #1 IC ORIENTATION

FAIRCHILD LIST OF MATERIAL

LM NO	-03	REV	QTY	UM	DESCRIPTION	NEXT ASSY	BY / DATE	CHK / DATE	MFG ENG / ENGR	DATE / DATE
					F8 KIT 2					

ITEM	PART NO	REV	QTY PER ASSM	U M	DESCRIPTION	REFERENCE DESIGNATION	CHANGE DOCUMENT REV	CHANGE DOCUMENT EN NO
1	3850DC		1		F-8 CPU			
2	3851ADC		1		F-8 PSU			
3	3853DC		1		F-8 SMI			
4	34001PC		1		QUAD-2 NOR	Q1		
5	34023PC		1		TRIPLE-3 NAND	Q2		
6	340097PC		2		TRI-STATE HEX BUFFER	Q3, Q4		
7	9N06PC		1		O.C. HEX BUFFER (INV.)	Q5		
8	34075PC		0		TRIPLE-3 OR (OPTIONAL)	Q6		
9	21022DC		8		1024-BIT RAM	D1-D8		
10	2N3904		1		TRANSISTOR, NPN (NOTE 1)	TR1		
11	2N3905		1		TRANSISTOR, PNP (NOTE 2)	TR2		
12	1N461A		1		DIODE, SILICON, G.P.			
					$I \geq 10MA @ V_R = 1.0V$ $B_V \geq 5V$ (NOTE 3)	CR1		
13	79PR20K		1		20K HELIPOT (BOURNS)	R4		
14			9		22K 1/4W 5% RESISTOR	R2, R9-R16		
15			5		6.8K 1/4W 5% RESISTOR	R1, R3, R5, R6, R8		
16			4		3.3K 1/4W 5% RESISTOR	R7, R21, R23, R24		
17			2		100Ω 1/2W 5% RESISTOR	R17, R18		
18			1		100Ω 1W 5% RESISTOR	R19 (IF 20MA TTY)		
			OR 1		1K 1/4W 5% RESISTOR	R19 (IF RS-232 TTY)		

** SUPPLIED IN KIT

DISHAR GRAPHICS/ACCUPRESS

FAIRCHILD LIST OF MATERIAL

LM NO	-03	REV	QTY	UM	DESCRIPTION	NEXT ASSY	BY ____ CHK ____ MFG ENG ____ DATE ____ DATE ____ DATE ____ ENGR ____ DATE ____

ITEM	PART NO	REV	QTY PER ASSM	U M	DESCRIPTION	REFERENCE DESIGNATION	CHANGE DOCUMENT REV	CHANGE DOCUMENT EN NO
19			1		1K ¼W 5% RESISTOR	R20 (ONLY IF 20MA TTY)		
20			1		270Ω ¼W 5% RESISTOR	R22		
21			1		SPDT P/B C&K 8121C;			
					8125C, OR EQUIV.	S1		
22			1		SPDT TOGGLE C&K7101-			
					SYC OR EQUIV.	S2		
23			1		CAP., MICA 10pF, 500V	C2		
24			1		CAP., CER. .47μF, 50V	C3		
					(ERIE 8131-050-651-.47-M)			
25			1		CAP. TANT. DIP. 4.7μF,	C1		
					35V SPRAGUE 196D475X	9035JA1 (OR EQUIV) (NOTE 4)		
26			1		CAP. TANT. DIP 47μF, 20V	C4		
					SPRAGUE 196D476X	9020PE4 (OR EQUIV.)		
27			1		CAP. TANT. DIP 100μF,	C5		
					10V SPRAGUE 196D107X	9010PE4 (OR EQUIV.)		
28			9		CAP. CER. .047μF, 50V	C6-C14		
					SPRAGUE 7C02347-3X050	(OR EQUIV.)		

BISHOP GRAPHICS/ACCUPRESS

FAIRCHILD LIST OF MATERIAL

LM NO	-03	REV	QTY	UM	DESCRIPTION	NEXT ASSY

BY _____ CHK _____ MFG ENG _____ DATE _____
DATE _____ DATE _____ ENGR _____ DATE _____

ITEM	PART NO	REV	QTY PER ASSM	U M	DESCRIPTION	REFERENCE DESIGNATION	CHANGE DOCUMENT REV	CHANGE DOCUMENT EN NO
					NOTES:			
					1. ITEM 10: SUBSTITUTE 2N3646			
					2. ITEM 11: SUBSTITUTE 2N5226, PN4916,			
					PN4917			
					3. ITEM 12: SUBSTITUTE ANY G.P. SILICON			
					DIODE MEETING MINIMUM SPECS GIVEN.			
					4. ITEMS 23-28: LISTED PART NO'S HAVE			
					.250 IN. LEAD SPACING. SUBSTITUTIONS ARE			
					DISCRETIONARY.			

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ERRATA

SEVERAL SHEETS ARE ENCLOSED TO ALERT SOLID STATE CUSTOMERS OF ANY ERRORS THAT HAVE BEEN FOUND IN FAIRCHILD DOCUMENTATION OR HARDWARE & TO UPDATE DOCUMENTATION.

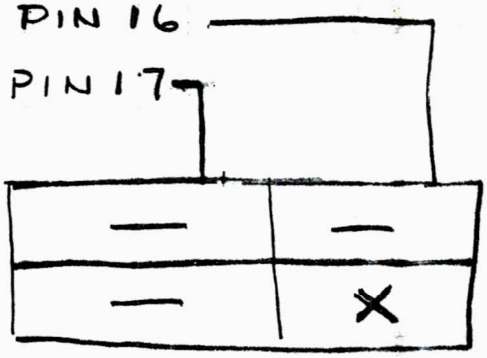
ITEM 1: APPENDIX H — "F8 DESIGN EVALUATION KIT".

PARAGRAPH 3.2 SHOULD READ; THE TTY CIRCUIT OPTION INVOLVES STRAPS J2, J3 & J4 & RESISTORS R19 & R20.

SEE FIGURE 1 - TTY OPTIONS (REVISED)

ITEM 2:

PARAGRAPH 4.2



110 BAUD

300 BAUD

(- = OPEN; X = TIE TO GND)

SYSTEM OPERATING SPEED SHOULD BE SET TO 2.0 MHz ± 5% (500 ns PERIOD) FOR CORRECT TELETYPE OPERATION: MONITOR THE 3850 PIN 1 WHILE ADJUSTING POT R4

EXECUTING A PROGRAM OUT OF FAIRBUG

IN ORDER TO EXECUTE A PROGRAM & RUN OUT OF FAIRBUG AT THE END OF THE USER'S PROGRAM THE NEXT 3 MEMORY LOCATIONS MUST BE INSTRUCTED TO JUMP OUT OF FAIRBUG THESE COMMANDS ARE 29, 80, 80. THEN SWITCH OUT OF FAIRBUG & RESET. THE PROGRAM HAS NOW BEEN EXECUTED.

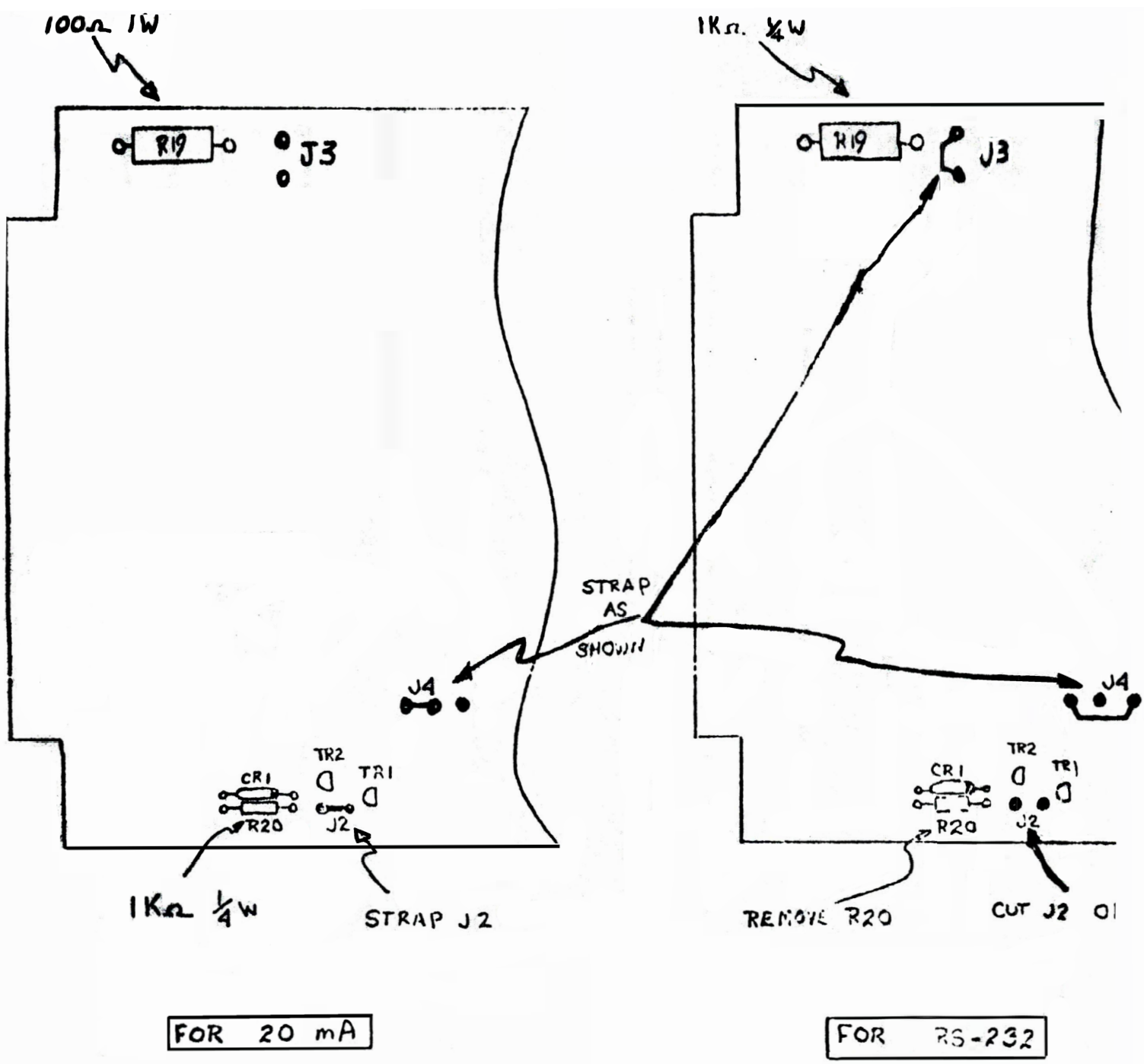


Figure 1 - TTY options

To date, five bugs have been discovered in the FAIRBUG program, none of which are catastrophic to the user. These bugs, which are all described below, are present in the 3851A PSU (SL31117), our current FAIRBUG.

Bug #1

Entry to FAIRBUG does not save the Status Register correctly; therefore, display of status is incorrect. Restoration of status when returning to USER is also incorrect. R9 is being used instead of status.

Upon entry to FAIRBUG a Disable Interrupt instruction is executed. Then R9 is stored to status; (instead of status being stored into R9 as desired). If Bit 4 of R9 is set, this effectively enables the interrupt system. Now, if an interrupt signal occurs, FAIRBUG will be interrupted back to the user.

In order to avoid this situation, the user should execute the following instructions before entering FAIRBUG:

```
DI ——— IA machine command ; Disable Interrupt
LR J,W—— IE machine command ; Store Status Register
```

This will result in the status now being correct, the interrupt being disabled, and R9 being destroyed.

Bug #2

This error is concerned with the premature termination of the display of blocks of memory upon execution of the "MXXXX-YYYY" FAIRBUG command. If the memory display terminates prior to reaching the desired location (YYYY in the above statement), the NEXT command can be used (up to 8 times may be required) to get past this premature termination point. Once into the next display block, another M or R command can be issued to continue the memory or register display to the desired final (YYYY) location.

Bug #3

This bug associates with the execution of the GO command in FAIRBUG. This bug results in registers R15, R14, R13, R9, IS, and W being incorrectly restored prior to returning to the user's program. If the user's program is being entered for the first time, or if he does not care about the restoration of these registers, then he needn't worry about this bug. If, however, FAIRBUG was entered via the user's program (say for the purpose of examining the status of some registers) and the user wishes to return to his program and continue execution where he left off, then the bug will give him erroneous results.

One partial solution to this bug can be achieved by execution of the FAIRBUG commands given below, prior to returning to the user's program. These will result in the proper restoration of all registers except R15 and R3B. While in FAIRBUG:

```
IS (IS)          Issue the commands to display the contents
R9 (R9)          of these registers and log their contents
W (W)            (       )
RD (RD)
RE (RE)
N                (moves pointer to R15)
C (RE)
RE
C (RD)           This alters the saved register values so that
R 3B             all but R15 will be restored correctly upon
C (IS)           execution of GO command)
N
C (R9)
N
C (W)
```

Bug #4

This minor bug exists which may occasionally prevent the user from executing the GO command immediately following a tape LOAD or tape PUNCH. If the user finds the GO command working incorrectly after the execution of tape LOAD or PUNCH, resetting FAIRBUG prior to executing GO will take care of this problem.

Bug #5

Scratchpad register 16 (R10) cannot be changed while in FAIRBUG. An attempt to do this will result in memory location 3FF (or BFF) being modified. Note that this RAM memory location is where the baud counter is stored on switch settings 10 and 11.

INPUT AND OUTPUT IN F8

The I/O system in the F8 family is simple to use. As there are two bi-directional I/O ports built into the F8 CPU and into each PSU, no additional hardware is necessary to generate the input/output pins to interface with external peripherals. Each I/O pin is a "wired-OR" structure between an internal latch and an external signal, if any, on this pin. As long as no external device puts an external signal on this pin, it behaves as a latched output. To use it in input mode, the latch should be cleared first by outputting a zero on this pin. Now any external signal connected to this pin can be read using Input instructions. Note that all I/O instructions use the CPUs accumulator as the principal source or destination register.

In addition to controlling I/O ports, I/O instructions are also used to transfer data between the accumulator and other programmable registers on some F8 circuits. For example, each PSU has two such registers: Timer and Interrupt Control Registers.

To avoid any malfunction, each I/O port and programmable register in the F8 system must have a unique address. Some of these addresses are dedicated, so it is a good idea to get familiar with the I/O map as early as you can. Also, the F8 instruction set allows short and long form input and output instructions. Short form commands are one-byte that implicitly address one of the first 16 ports in the system. Long form commands are two byte instructions. Since the second byte contains a full 8-bit I/O address, hence, there are 256 different addresses available in an F8 system.

Addresses Ø and 1 are assigned to the I/O ports on the F8 CPU. Each PSU has a programmable mask option for the upper six bits [Note: This mask is different from the six bits of Page Select] of the I/O addresses. The four registers on PSU are assigned in the following sequence:

X X X X X X	00	I/O Ports
X X X X X X	01	
X X X X X X	10	Interrupt Control Register
X X X X X X	11	Timer Register

Note: To avoid confusion with the CPU ports, this cannot be all 0's.

In the case of the 3852 and 3853 MI circuits, addresses B'00001100', B'00001101', B'00001110', and B'00001111' are dedicated for the internal registers. [Refer to INTERRUPTS and MI Specifications]. Four of the highest numbered addresses in the system are dedicated to the DMA control functions. The exact four are chosen at the time of installation by hard-wiring two select pins on the DMA chip. However they will always fall in one of the last four sets. [H'F0'-H'F3', H'F4'-H'F7', H'F8'-H'FB', or H'FC'-H'FF'].

A recent addition to the F8 family is the 3820 Peripheral Interface Adapter. This is a general-purpose I/O component which permits users to separate I/O and memory functions when it is more convenient to do so. PIAs will normally be addressed like ordinary memory locations, and will accordingly be supported by one of the standard memory interfaces. The programming of these devices can get involved, and lies outside the scope of this introduction. Refer to the individual spec sheet for full details.

THE FOLLOWING IS A SHORT PROGRAM WHICH REQUIRE 24 BYTES OF RAM MEMORY.
THE FIRST 16 BYTES ARE INSTRUCTINS WHICH ARE USED TO CHANGE THE NEXT 8 BYTES IN RAM TO (88)

```
        M0
        M0000=C1
CHANGE ——?C1B ———— ENABLE INTERRUPT
NEXT ——?N M0001=F3
        ?C20 ———— LOAD ACC IMMED,
        ?N M0002=39
        ?C08 ———— STORE STACK REGISTER
        ?N M0003=FE
        ?C50 ———— NON INSTRUCTION
        ?N M0004=6F
        ?C2A ———— LOAD DATA COUNTER IMMED.
        ?N M0005=FE
        ?C00 ———— LR A,KU  ACC ← (↑12)
        ?N M0006=FD
        ?C10 ———— LOAD DATA COUNTER
        ?N M0007=FB
        ?C20 ———— LOAD ACC IMMED
        ?N M0008=FF
        ?C88 ———— NUMERIC FOR BYTES # 17-24
        ?N M0009=76
        ?C17 ———— STORE
        ?N M000A=00
        ?C30 ———— NON INSTRUCTION
        ?N M000B=00
        ?C94 ———— BRANCH IF NOT ZERO
        ?N M000C=80
        ?CFB ———— CORRECT BNZ INSTRUCTION
        ?N M000D=8A
        ?C29 ———— JUMP
        ?N M000E=3E
        ?C80 ————
        ?N M000F=C4          } INSTRUCTION TO OPERATE OUT OF FAIRBUG & STILL
        ?C80 ————              USER SERIAL PORT # 4
        ?M0-10
         M0000=1B 20 08 50 2A 00 10 20 }
         M0008=88 17 30 94 FB 29 80 80 } EXAMINE MEMORY LOCATIONS
         M0010=00 00 00 00 00 00 00 00 } M0-10 (DECIMAL 0-24)
        ?—TOGGLE SWITCH OUT OF FAIRBUG.
        ?
        ?—EXECUTE MANUAL RESET
        ?M0-10
         M0000=1B 20 08 50 2A 00 10 20 }
         M0008=88 17 30 94 FB 29 80 80 } PROGRAM EXECUTED: REEXAMINE
         M0010=88 88 88 88 88 88 88 88 } M0-10
```